## CLAIMS

What is claimed is:

1. A mixed signal circuit comprising:

a plurality of fixed threshold and variable threshold transistors;

a plurality of Schottky barrier diodes;

a plurality of poly silicon film resistors;

a plurality of capacitors; and

a plurality of wiring tracks, wherein all of the elements are on a single substrate to form integrated circuits with implementing macro functions.

2. The mixed signal circuit of claim 1 wherein the circuit is software driven.

3. The mixed signal circuit of claim 2 wherein software is provided to adjust the threshold of the variable threshold transistors.

4. The mixed signal circuit of claim 2 wherein software is provided to form reconfigurable logic gate array circuit units.

5. The mixed signal circuit of claim 2 wherein software is provided to complete certain network connections among various units in the single diagram.

6. The mixed signal circuit of claim 2 wherein the software includes state tables, virtual machines, setup or initialization and test procedures, data access, transport, and storage algorithms.

7. The mixed signal circuit of claim 1 wherein the circuit is hardware driven, wherein the hardware comprises hardwired Schottky CMOS Logic (SCL) gate array and memory units, IO transceivers, and terminators.

8. The mixed signal circuit of claim 7 wherein the hardware comprises software driven SCL gate arrays, IO transceivers, terminators, capacitors and wherein a switch transistor is of VT type.

9. The mixed signal circuit of claim 7 which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL unit act as analog signal comparator.

10. The mixed signal circuit of claim 7 which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL gate may perform a nonvolatile latch function.

11. The mixed signal circuit of claim 7 which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type,

and the SCL unit may process multi-value logic operation with binary, ternary and quaternary operators.

12. The mixed signal circuit of claim 7 which includes software driven CMOS-TTL gate arrays, IO transceivers, terminators and capacitors.

13. The mixed signal circuit of claim 7 which includes hardwired conventional logic and memory units including but not limited to CMOS-TTL gate arrays, Register files, embedded RAM, ROM and Flash cores.

14. The mixed signal circuit of claim 7 which includes dedicated programming facilities of voltage and current sources, clock and oscillators, state machines and counters, to implement and control both cell wise and block wise cell operations and which is shared to alter the charge storage or VT threshold of the selected device(s) in the logic and (Flash) memory circuitry.

15. The mixed signal circuit of claim 1 wherein the SBDs comprise a PN junction diode if SOI GaAs technologies are used.

16. The mixed signal circuit of claim 1 wherein the SBD can be coupled to input pads for Electrical Static Discharge protection.

17. The mixed signal circuit of claim 1 wherein the SBD can be coupled to the well for Latch-up suppression.

18. The mixed signal circuit of claim 1 wherein the SBD can be coupled to control the well biasing potential, therefore change I-V characteristics of CFETs within the well region with circuit operating conditions.

19. The mixed signal circuit of claim 3 wherein the SBDs are adaptable to other product applications including but not limited to DRAM, Flash, CAM, PLD, ROM, and embedded ASICs.

20. A mixed signal circuit comprising:

a plurality of fixed threshold and variable threshold transistors;

a plurality of Schottky barrier diodes;

a plurality of poly silicon film resistors;

a plurality of capacitors; and

a plurality of wiring tracks, wherein all of the elements are on a single substrate to form integrated circuits with implementing macro functions, wherein the circuit is software driven and wherein the at least a portion of the macro functions can be hardwired macroassets.

21. The mixed signal circuit of claim 20 wherein software is provided to adjust the threshold of the variable threshold transistors.

22. The mixed signal circuit of claim 20 wherein software is provided to form reconfigurable logic gate array circuit units.

23. The mixed signal circuit of claim 20 wherein software is provided to complete certain network connections among various units in the single diagram.

24. The mixed signal circuit of claim 20 wherein the software includes state tables, virtual machines, setup or initialization and test procedures, data access, transport and storage algorithms.

25. The mixed signal circuit of claim 20 wherein the circuit is hardware driven, wherein the hardware comprises hardwired Schottky CMOS Logic (SCL) gate array and memory units, IO transceivers, and terminators.

26. The mixed signal circuit of claim 25 wherein the hardware comprises software driven SCL gate arrays, IO transceivers, terminators, capacitors and wherein a switch transistor is of VT type.

27. The mixed signal circuit of claim 25 which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL unit act as analog signal comparator.

28. The mixed signal circuit of claim 25, which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL gate may perform a nonvolatile latch function.

29. The mixed signal circuit of claim 25 which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL unit may process multi-value logic operation with binary, ternary and quaternary operators.

30. The mixed signal circuit of claim 25 which includes software driven CMOS-TTL gate arrays, IO transceivers, terminators and capacitors.

31. The mixed signal circuit of claim 25 which includes hardwired conventional logic and memory units including but not limited to CMOS-TTL gate arrays, Register files, embedded RAM, ROM and Flash cores.

32. The mixed signal circuit of claim 25 which includes dedicated programming facilities of voltage and current sources, clock and oscillators, state machines and counters, to implement and control both cell wise and block wise cell operations and which is shared to alter the charge storage or VT threshold of the selected device(s) in the logic and (Flash) memory circuitry.

33. A mixed signal circuit comprising:

a plurality of fixed threshold and variable threshold transistors;

a plurality of Schottky barrier diodes;

a plurality of poly silicon film resistors;

a plurality of capacitors; and

a plurality of wiring tracks, wherein all the elements are on a single substrate to form integrated circuits with implementing macro functions, wherein a part of the elements are user programmed and part of the elements are factory programmable, wherein the circuit is software driven.

34. The mixed signal circuit of claim 33 wherein software is provided to adjust the threshold of the variable threshold transistors.

35. The mixed signal circuit of claim 33 wherein software is provided to form reconfigurable logic gate array circuit units.

36. The mixed signal circuit of claim 33 wherein software is provided to complete certain network connections among various units in the single diagram.

37. The mixed signal circuit of claim 33 wherein the software includes state tables, virtual machines, setup or initialization and test procedures, data access, transport, and storage algorithms.

38. The mixed signal circuit of claim 33 wherein the circuit is hardware driven, wherein the memory comprises hardwired Schottky CMOS Logic (SCL) gate array and memory units, IO transceivers, and terminators.

39. The mixed signal circuit of claim 38 wherein the hardware comprises software driven SCL gate arrays, IO transceivers, terminators, capacitors and wherein a switch transistor is of VT type.

40. The mixed signal circuit of claim 38 which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL unit act as analog signal comparator.

41. The mixed signal circuit of claim 38 which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL gate may perform a nonvolatile latch function.

42. The mixed signal circuit of claim 38 which includes software driven SCL gate arrays, IO transceivers, terminators, capacitors, wherein the switch transistor is of VT type, and the SCL unit may process multi-value logic operation with binary, ternary and quaternary operators.

43. The mixed signal circuit of claim 38 which includes software driven CMOS-TTL gate arrays, IO transceivers, terminators and capacitors.